Chapter 19
Configure EIA-530 Interfaces

Devices that communicate over a serial interface are divided into two classes: data terminal equipment (DTE) and data circuit-terminating equipment (DCE). EIA-530 is an Electronics Industries Alliance (EIA) standard for the interconnection of DTE and DCE employing serial binary data interchange with control information exchanged on separate control circuits. Juniper Networks EIA-530 Physical Interface Cards (PICs) have two ports per PIC and support full-duplex data transmission. These PICs support DTE mode only.

The following standards apply to EIA-530 interfaces:

TIA/EIA Standard 530, *High-Speed 25-P osition Interf ace f or Dat a Terminal Equipment and Dat a Circuit-Terminating Equipment* , defines the signals on the cable and specifies the connector at the end of the cable.

TIA/EIA Standard 232, *Interface betw een Dat a Terminal Equipment and Dat a Circuit-Terminating Equipment Emplo ying Serial Binary Data Interchange*, describes the physical interface and protocol for serial data communication.

To configure EIA-530 physical interface properties, include the serial-options statement at the [edit interfaces ei-*fpc*/*pic*/*port*] hierarchy level:

```
[edit interfaces ei-fpc/pic/port]
serial-options {
    clock-rate rate;
    clocking-mode (dce | dte | loop);
    control-leads {
        cts (ignore | normal | require);
        dcd (ignore | normal | require);
        dsr (ignore | normal | require);
        dtr (assert | auto-synchronize | de-assert | normal);
        ignore-all;
        rts (assert | de-assert | normal);
        tm (ignore | normal | require);
    }
    cts-polarity (positive | negative);
    dcd-polarity (positive | negative);
    dsr-polarity (positive | negative);
    dtr-circuit (balanced | unbalanced);
    dtr-polarity (positive | negative);
    encoding (nrz | nrzi);
    loopback (dce-local | dce-remote | liu | local);
    rts-polarity (positive | negative);
    tm-polarity (positive | negative);
    transmit-clock invert;
}
```

This chapter discusses configuration of the following EIA-530 interface properties:

There are no EIA-530 interface-specific logical properties. For information about general logical properties that you can configure, see “Configure Logical Interface Properties” on page 63.

Configure the EIA-530 Clocking Mode

You can configure each port on the PIC independently to use DCE, loop, or DTE clocking mode:

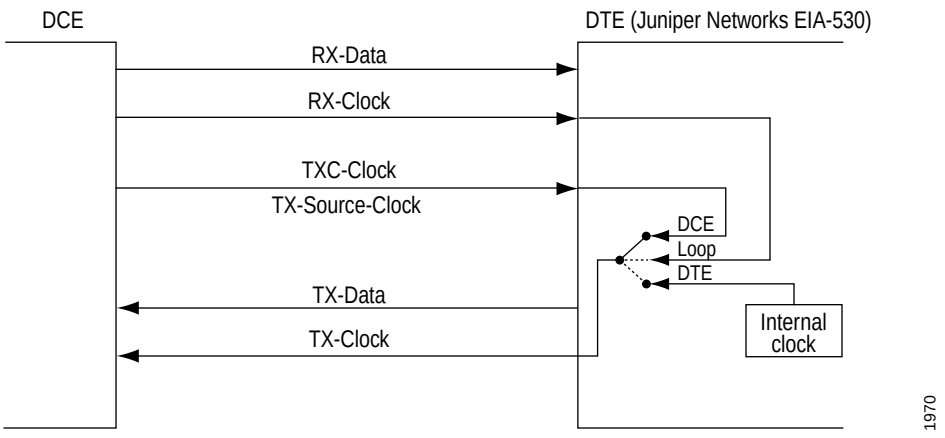
DCE clocking mode—Uses the TXC clock, which is generated by the DCE specifically to be used by the DTE as the DTE’s transmit clock.

Loop clocking mode—Uses the DCE’s RX clock to clock data from the DCE to the DTE.

DTE clocking mode—Also known as line timing, uses an internally generated clock. You can configure the speed of this clock by including the clock-rate statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level. For more information about the DTE clock rate, see “Configure the DTE Clock Rate” on page 223.

Note that DCE clocking mode and loop clocking mode use external clocks generated by the DCE. Figure 19 shows the clock sources of DCE, loop, and DTE clocking modes.

Figure 19: EIA-530 Interface Clocking Mode



To configure the clocking mode of an EIA-530 interface, include the clocking-mode statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
clocking-mode (dce | dte | loop);
```

Invert the EIA-530 Interface Transmit Clock

When an externally timed clocking mode (DCE or loop) is used, long cables might introduce a phase shift of the DTE-transmitted clock and data. At high speeds, this phase shift might cause errors. Inverting the transmit clock corrects the phase shift, thereby reducing error rates.

To invert the transmit clock, include the transmit-clock invert statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
transmit-clock invert;
```

Configure the DTE Clock Rate

When you configure the clocking mode to be DTE, you can configure the interface speed for the EIA-530 interface. By default, the EIA-530 interface has a signaling speed of 16.384 MHz. To configure the interface speed, include the clock-rate statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
clock-rate rate;
```

You can configure the following interface speeds:

2.048mhz—2.048 MHz

2.341mhz—2.341 MHz

2.731mhz—2.731 MHz

3.277mhz—3.277 MHz

4.096mhz—4.096 MHz

5.461mhz—5.461 MHz

8.192mhz—8.192 MHz

16.384mhz—16.384 MHz

Although the EIA-530 interface is intended for use at the default rate of 16.384 MHz, you might need to use a lower rate if any of the following conditions prevail:

The interconnecting cable is too long for effective operation.

The interconnecting cable is exposed to an extraneous noise source that might cause an unwanted voltage in excess of + 1 volt measured differentially between the signal conductor and circuit common at the load end of the cable, with a 50 ohm resistor substituted for the generator.

You need to minimize interference with other signals.

You need to invert signals.

For detailed information about the relationship between signaling rate and interface cable distance, see the following standards:

EIA-422-A, *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*

EIA-423-A, *Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits*

Configure the EIA-530 Signal Handling

You can configure EIA-530 signal characteristics by including the control-leads statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
control-leads {
    cts (ignore | normal | require);
    dcd (ignore | normal | require);
    dsr (ignore | normal | require);
    dtr (assert | auto-synchronize | de-assert | normal);
    ignore-all;
    rts (assert | de-assert | normal);
    tm (ignore | normal | require);
}
```

Assertion is when the (+ side) of a given signal is at potential high-level output voltage (Voh), while the (– side) of the same signal is at potential low-level output voltage (Vol). *Deassertion* is when the (+ side) of a given signal is at potential Vol, while the (– side) of the same signal is at potential Voh.

To-DCE signals include data-transfer-ready (DTR) and request-to-send (RTS) signals. For the DTR and RTS signals, if you include the assert statement in the configuration, the to-DCE signal must be asserted. If you include the de-assert statement in the configuration, the to-DCE signal must be deasserted.

For the DTR signal, you can configure normal signal handling with automatic synchronization using the signal for resynchronization by including the auto-synchronize statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options control-leads dtr] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options control-leads dtr]
auto-synchronize {
    duration milliseconds;
    interval seconds;
}
```

The pulse duration of resynchronization can be from 1 through 1000 milliseconds.

The offset interval for resynchronization can be from 1 through 31 seconds.

From-DCE signals include the clear-to-send (CTS), data-carrier-detect (DCD), data-set-ready (DSR), and test-mode (TM) signals. For the CTS, DCD, DSR, and TM signals, if you include the require statement in the configuration, the from-DCE signal is asserted. If you include the ignore statement in the configuration, the from-DCE signal is ignored.

For each signal, the normal option applies to the normal signal handling for that signal, as defined by the TIA/EIA Standard 530. By default, normal signal handling is enabled for all signals. To return to the default normal signal handling, delete the require, ignore, assert, de-assert, or auto-synchronize statement from the configuration, as shown in the following examples:

```
[edit]
user@host# delete interfaces ei-0/1/0 serial-options control-leads cts require

[edit]
user@host# delete interfaces ei-0/1/0 serial-options control-leads rts assert

[edit]
user@host# delete interfaces ei-0/1/0 serial-options control-leads dtr autosynchronize

[edit]
user@host# delete interfaces ei-0/0/0 serial-options control-leads rts de-assert

[edit]
user@host# delete interfaces ei-0/0/0 serial-options control-leads cts ignore
...
```

To explicitly configure normal signal handling, include the normal statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options control-leads (cts | dcd | dsr | dtr | rts | tm)] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options control-leads cts]
normal;
```

You can configure the EIA-530 interface to ignore all control leads by including the ignore-all statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options control-leads] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options control-leads]
ignore-all;
```

You can include the ignore-all statement in the configuration only if you do not explicitly enable other signal handling options at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options control-leads] hierarchy level.

Configure the EIA-530 DTR Circuit

A balanced circuit has two currents that are equal in magnitude and opposite in phase. An unbalanced circuit has one current and a ground; if a pair of terminals is unbalanced, one side is connected to electrical ground and the other carries the signal. By default, the DTR circuit is balanced.

To configure the DTR circuit on an EIA-530 interface, include the dtr-circuit statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
dtr-circuit (balanced | unbalanced);
```

Configure EIA-530 Signal Polarities

EIA-530 interfaces use a differential protocol signaling technique. Of the two EIA signals associated with a circuit, the one referred to as the A signal is denoted with a plus sign, and the one referred to as the B signal is denoted with a minus sign; for example, DTR + and DTR–. If DTR is low, then DTR + is negative with respect to DTR–. If DTR is high, then DTR + is positive with respect to DTR–. By default, all signal polarities are positive.

You can reverse this polarity on a Juniper Networks EIA-530 interface. You might need to do this if signals are miswired as a result of reversed polarities.

To configure signal polarities on an EIA-530 interface, include the cts-polarity, dcd-polarity, dsr-polarity, dtr-polarity, rts-polarity, and tm-polarity statements at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
cts-polarity (positive | negative);
dcd-polarity (positive | negative);
dsr-polarity (positive | negative);
dtr-polarity (positive | negative);
rts-polarity (positive | negative);
tm-polarity (positive | negative);
```

Configure EIA-530 Loopback Capability

To configure the loopback capability on an EIA-530 interface, include the loopback statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces ei-fpc/pic/port serial-options]
loopback (dce-local | dce-remote | liu | local);
```

To determine the source of a problem, you can loop packets on the local router, the local DCE, the remote DCE, and the line interface unit (LIU). To do this, include the no-keepalives and encapsulation cisco-hdlc statements at the [edit interfaces ei-*fpc*/*pic*/*port*] hierarchy level, and the loopback local option at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level:

```
[edit interfaces]
ei-1/0/0 {
    no-keepalives;
    encapsulation cisco-hdlc;
    serial-options {
        loopback local;
    }
    unit 0 {
        family inet {
            address 100.100.100.1/24;
        }
    }
}
```

With this configuration, the link stays up, so you can loop ping packets to a remote router. The loopback local statement causes the interface to loop within the PIC just before the data reaches the transceiver. You can determine whether there is an internal or external problem by checking the error counters in the output of the show interface ei-*fpc*/*pic*/*port* extensive command:

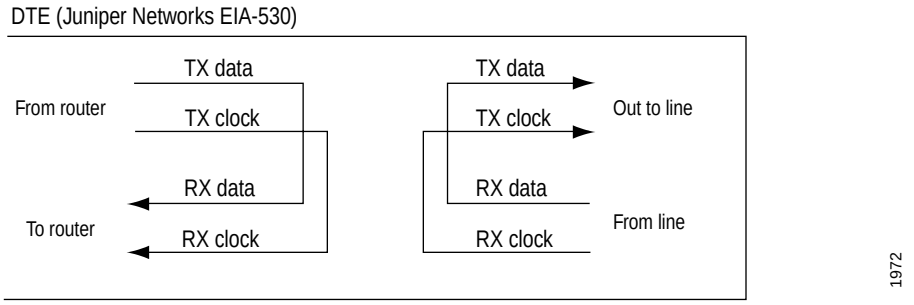
```
> show interfaces ei-1/0/0 extensive
```

To turn off the loopback capability, remove the loopback statement from the configuration:

```
[edit]
user@host# delete interfaces ei-1/0/0 serial-options loopback
```

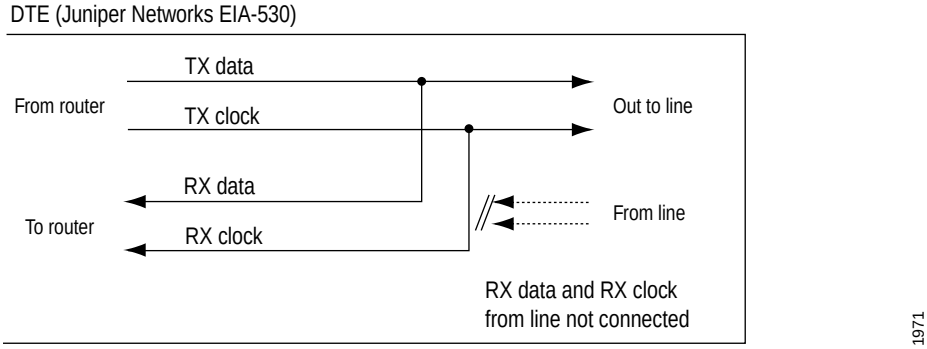
From the router, LIU loopback loops the TX (transmit) data and TX clock back to the router as RX (receive) data and RX clock. From the line, LIU loopback loops the RX data and RX clock back out the line as TX data and TX clock, as shown in Figure 20.

Figure 20: EIA-530 Interface LIU Loopback



DCE local and DCE remote control the EIA-530 interface-specific signals for enabling local and remote loopback on the link partner DCE. Local loopback is shown in Figure 21.

Figure 21: EIA-530 Interface Local Loopback



Configure EIA-530 Line Encoding

By default, EIA-530 interfaces use non-return to zero (NRZ) line encoding. You can configure non-return to zero inverted (NRZI) line encoding if necessary.

To have the interface use NRZI line encoding, include the encoding statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level, specifying the nrzi option:

```
[edit interfaces ei-fpc/pic/port serial-options]
encoding nrzi;
```

To explicitly configure the default NRZ line encoding, include the encoding statement at the [edit interfaces ei-*fpc*/*pic*/*port* serial-options] hierarchy level, specifying the nrz option:

```
[edit interfaces ei-fpc/pic/port serial-options]
encoding nrz;
```

When setting the line encoding parameter, you must set the same value for paired ports. Ports 0 and 1 must share the same value.